ISSN: 2582 - 6379
Orange Publications
International Journal for Interdisciplinary Sciences and Engineering Applications
IJISEA - An International Peer- Reviewed Journal
2023, Dec, Volume 4 Issue 4
www.ijisea.org

Low-Power RHBD 12T SRAM with Multi-Node Upset Recoverability for Aerospace Applications

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ABSTRACT

Based on the physical mechanism of upset in soft mistakes and a practical layout-topology, a new radiation-hardened-by-design (RHBD) 12T storage location is presented. The acquired verification findings show that the suggested 12T cell has the potential to deliver excellent radiation resistance. In comparison to a 13T cell, the proposed 12T cell has space (18.9%), power (23.8%), and read/write access time (171.6%) overheads. It has a greater hold static noise margin than a 13T cell, at 986.2 mV. Since the suggested 12T cell also has the potential to tolerate faults, it is more stable.CMOS technology plays an important role in the modern electronics world. CMOS technology also plays significant role in aerospace applications. To store data, memories are widely used as the medium in aerospace applications. SRAM cells are the memories made by the CMOS technology. The most vital issues faced by memories are due to single event upsets (SEUs) which are induced by radiation particles. The SEU's due to increase in densities and SEU's. There is a decrease in critical charge and supply voltage in CMOS process technology. There is a need for a technique which can to tolerate these SEU's in such aerospace applications. Which are in the environment of complex celestial radiation? The technique which is considered for such environment is radiation-hardened by design (RHBD) with soft error robustness. This paper aims at is proposing an area efficient and high reliable RHBD memory cell.

Keywords: RHBD , CMOS Technology, Memory Cell , layout Design

I.INTRODUCTION

The proliferation of demand for low energy devices such as wireless sensor networks, implantable medical imaging and other portable devices powered by batteries has contributed to a major design restriction for dissipation. The Static Access Memory, which occupies large proportions of Systems-on-Chip (SoCs) and its application, is the main contributor to the power dissipation.

In the future, the portion will begin to grow[1]. Moreover, leakage is becoming a major threat with the introduction of ultra-scale technology. As the leakage rise exponentially, threshlal voltage (TH) reduction and gate-oxide thickness increase the power consumption[2]. In order to provide a resource efficient architecture, it is also important to minimise the power associated with SRAM. Easy means to gain power reliability by reducing voltage supply because of quadratically and exponentially decreased power and leakage pressure with voltage supply[3] respectively. But process variance significantly degrades SRAM

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cell output at lower supply voltages[4]. As a consequence of the difficulties of preserving the system intensity ratio in the sub-threshold region[5], the likelihood of read/write loss in traditional 6T S RAM is dramatically increased.

Several combinations of SRAM cells[6]-[13] have been suggested by the researchers to address read loss by a separate read buffer. The static range read (RSNM) of these cells is improved by decoupling the read/write route but still has a weak written margin (WM) in the sub-threshold region. In comparison, the literature documenting different writing-help strategies to raise the SRAM cell compose margin [14]-[20]. Boosting the Word-line [14], [15] and negative bitline (NBL) [16] are the traditionally implemented writing assistance techniques that improve the writeability of a write access transistor by enhancing its driving power. These methods, though, contribute to region and power fines. Another effective approach to increase writability is to weaken the power of the interconnection inverter pair. It protects power cuts [17], [18], [19] rises or [11] floats, [20] VSS cells, etc.

II.LITERATURE SURVEY

A.STATIC RAM:

The term static indicates that the memory holds its contents as electricity is supplied. But, as the power slips because of its instability, data is lost. SRAM chips have a 6- transistor matrix with no condensers. SRAM should not be periodically updated with transistors to avoid leakage.

The matrix requires more room, and SRAM needs more chips than DRAM with the same volume of capacity, rendering processing costs more costly. Thus, SRAM has very fast access to cache memory.

The memory circuit is considered to be permanent because the data processed can be held forever without a daily refresh operation (as long as there is ample power voltage available). The configuration of the circuit and the activity of basic SRAM cells as well as the peripherals to read and write the data are studied.

A single lock circuit, two secure operating points (states), often comprises of the data processing cell, i.e. the 1-bit memory cell of static RAM arrays. The records that are in Memory cell are represented either as a logic "0" or as a logic "1," based on the retained state of the two inverter lock circuits. To reach and re-read the data in the memory cell over the memory bit line, at least a one switch is required, that is to say the row address selection signal (Fig 2.1(a). For most instances the 1-bit SRAM cell is wired to the complementary bit lines (columns) with two complimentary control switches made up from the NMOS transistor transfers. It is equivalent to rotating the steering wheel in different ways in both left and right sides.

B.6T-SRAMTOPOLOGY:

In computerized circuit, two cross coupled inverters are treated as a memory component called as a latch. In 6T-SRAM there are two additional doors called as a pass entryways constrained by word line terminal, which are utilized for getting to of information from memory component or compose the information in to memory component through bit line, bit line bar ports. The 6T SRAM geography is as per the following.

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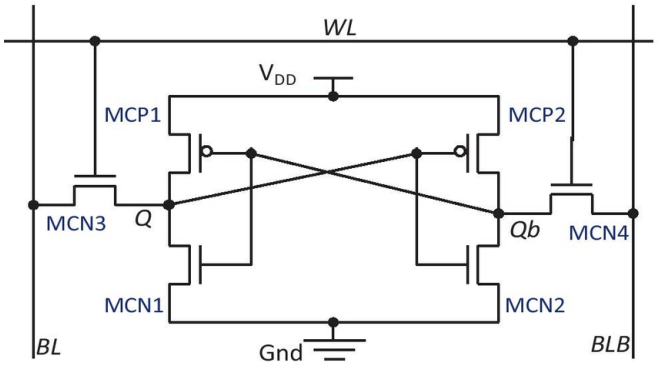

Fig 1: Shows 6T-SRAM Topology

III.PROPOSED SRAM CELL

Memories play a crucial role in today's circuit designs. SRAM is an integral part of many different electronic systems that serve as memory. SRAMs were developed with lower latency, smaller footprint, less power consumption, and higher dependability in mind [1]. High densities, a low critical charge, and a low supply voltage often have a significant impact on the dependability of SRAM cells. Single event upset may develop when a particle hits an SRAM cell and alters the cell's state. SRAMs' use of active particles aids in their struggle against reliability triggering. Single event upsets (SEUs) are a kind of failure mechanism that may cause electronic devices to malfunction by briefly altering the charge that has been stored in them [2]. An instantaneous voltage spike is produced. After a node's stored value has been changed. The 6T SRAM cell is typically constructed using move-coupled inverters. When a mistake occurs in the memory, causing data overwriting and faults, the charge which is formed in the stored node might initiate observations process, in order to turn the domain in some other responsive node [3-4]. Increases in density, decreases in critical charge, and shrinking feature sizes are all characteristics of the CMOS process that make SRAM cells more susceptible to this reliability challenge. Manuscript, Revised Accepted on or around August 5, 2019 by M. Chaitanya, Postgraduate Student at GMR Institute of Technology, India V. Kannan is a professor in the Electrical and Computer Engineering (ECE) department of GMRIT in Rajam, India. reduce the input voltage [1]. The aerospace industry relies heavily on radiation-hardened by-design (RHBD) procedures since they are purpose-built for extreme conditions. Conventional SEU memory architectures, such as the 10T memory cell, are able to withstand single event upsets, but not many event upsets at once [7]. 12T memory cells have been offered as a solution to the problem of repeated event upsets; they are effective in high radiation conditions, but they also need more energy to operate [8].

Depending on the information stored on QB, the RBL discharge route is set to transistor MR1 and MR2. The WLA and WLB signals may be deleted from every read trouble route while read Access allows for full separation of the data storage nodes (Q and QB). Except for sub-threshold operations, the "interpret disturbed" is thus of no importance. In Keep Mode, all of the control signals are deactivated and the inverters may be fully separated without a floating node. The cell stability in keeping mode is also similar to the 6T cell. The VVSS signal stays strong, reducing static electricity usage dramatically during standby.

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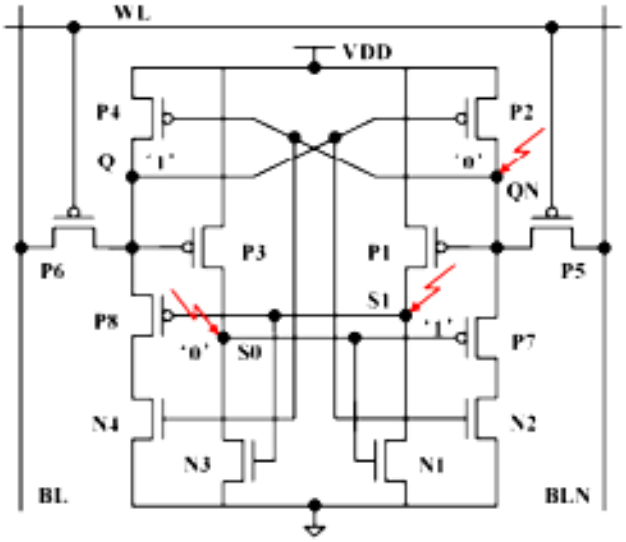

Fig 2: Shows Proposed RHBD 12T Memory Cell

For a long time now, regular commercial CMOS foundry methods have been utilised in conjunction with radiation-hardening-by-design (RHBD) approaches to accept soft mistakes in memory without requiring any changes to the current process or violation of design standards [6]. In general, these methods may be broken down into the following three categories. For radiation tolerance, 1) Layout-level approaches rely heavily on layout modifications such H-gates, T-gates, annular gates, and shallow trench isolation (STI) [8, 9]. While it's true that layout-level approaches may provide some security, doing so with nanoscale technologies is challenging because to stricter design requirements. When it comes to protecting against SEU in memory and latches, the first circuit-level method is triple modular redundancy (TMR) [10]. This protection method uses a voting circuit to identify the correct output from three identical memory cells storing the same data. Even if disruption occurs in one cell, the other two copies will retain their original state. The majority voting procedure is then put into action to ensure the correct output of the stored data. TMR's primary drawback is the enormous area overrun and power dissipation it necessitates [11]. When hardening a circuit, it's usual practise to either propose new toughened memory cells or add redundant transistor based on the regular 6T cell. The 10T toughened memory cell suggested by Jahinuzzaman et al. [12] uses ten transistors. But it can only restore 1 0 SEU. In [13], it is suggested that PS-10T and NS-10T toughened memory cells only provide limited SEU resistance. To rephrase, a PS-10T cell is limited to recovering 1 0 SEU, whereas an NS-10T cell can only do so for a total of 1 SEU. Using a total of 12 transistors, the dual interlocked storage cell (DICE) is presented in [14] to provide fault resilience at a single node. Using a single-ended memory structure, 11T cells are suggested recently [15, 16]. In 13T cell, the hysteresis effect of the Schmitt trigger causes the sharing critical charge to be somewhat higher than in 11T cell. In order to offer a novel, more robust memory cell, Rajaei et al. [17] have refined the construction of a 13T memory cell (R13T). The critical charge sharing in R13T cell is higher than in 13T cell. However, these cells' primary weakness is that they are unable to survive a disruption involving numerous nodes at once. In [9], a multiple-node upset-tolerant RHD12T memory cell is presented by combining a circuit-level hardening strategy with a layout-level STI approach. This memory cell, however, has a larger area overhead and less stability than others. Thirdly, the use of error correction codes (ECCs) in the system-level design allows for a greater margin of error tolerance. Since the encoding and decoding circuits are more sophisticated, ECC approaches would need greater overheads, notably for temporal performance (nanosecondlevel delay) [21] - [24]. As a result, memory's real-time performance will suffer greatly. In

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general, circuit-level RHBD memory design has the benefit of providing not only stronger fault tolerance capability, but also reduced overheads, notably for time performance, as compared to hardening strategies at the layout and system levels (Pico second-level delay). Here, we propose a new RHBD 12T cell at the circuit level to increase memory's resistance to SEUs.

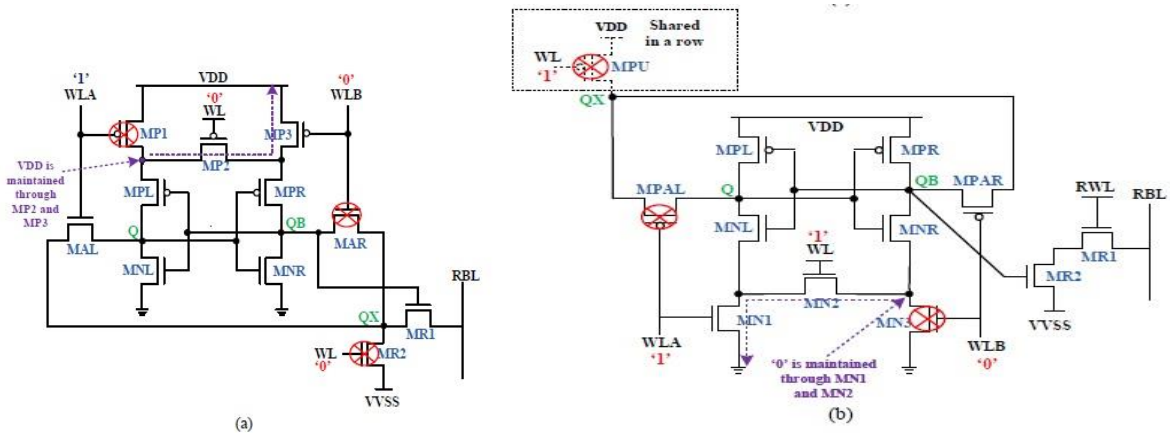
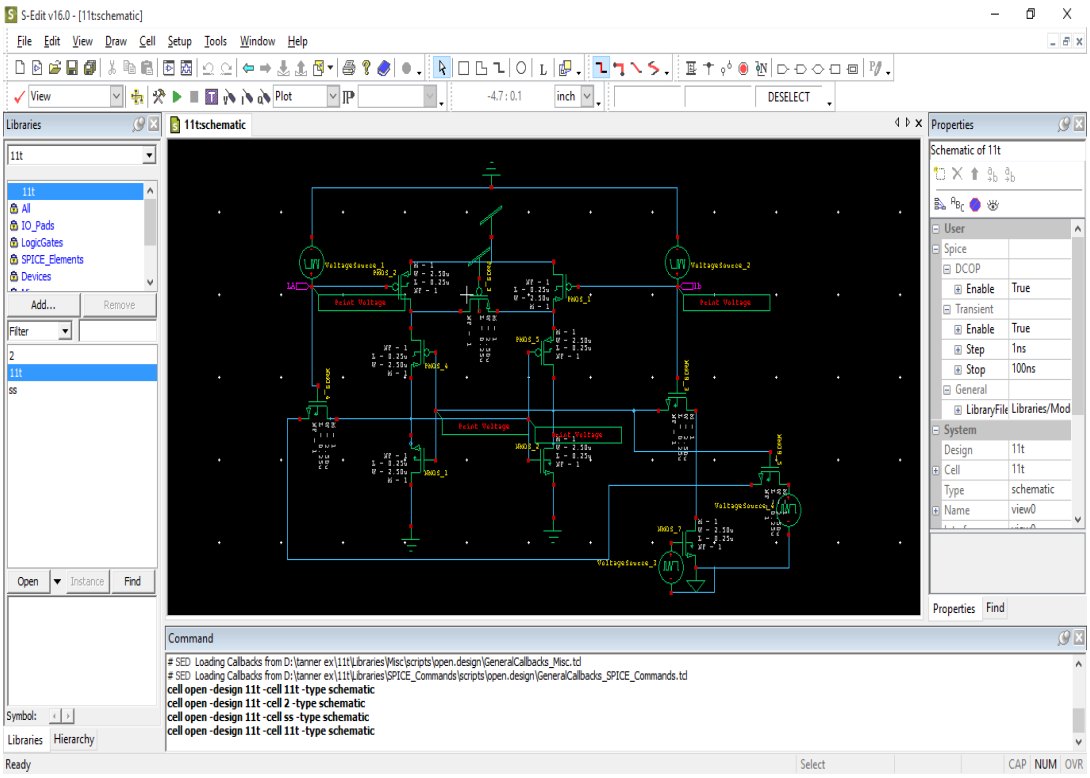


Fig 3 : Column Half Select cell Under write '0' operation in (a)11T-1 (b)11T-2 cell

IV. RESULTS AND DISCUSSION

Existing Method Schematic:



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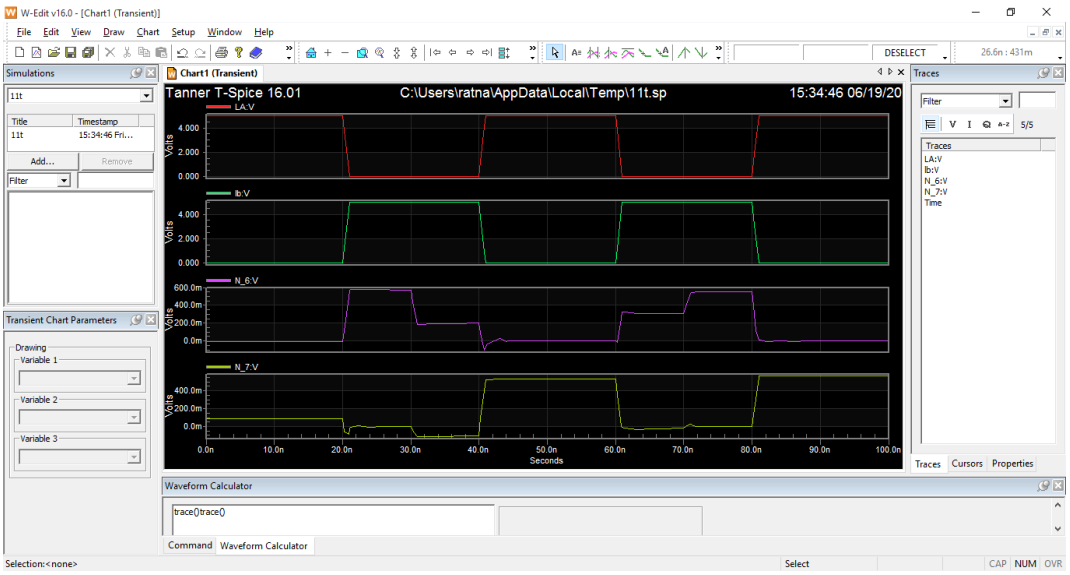
Waveform:




```
Device and node counts:
            MOSFETs -       11
   MOSFET geometries -        2
     Voltage sources -        4
         Subcircuits -        0
   Model Definitions -        2
     Computed Models -        2
   Independent nodes -        9
      Boundary nodes -        5
         Total nodes -       14
```

(a)

```
Parsing                    0.06 seconds
Setup                      0.05 seconds
DC operating point         0.06 seconds
Transient Analysis         0.01 seconds
Overhead                   0.97 seconds
-----------------------------------------
Total                      1.15 seconds
```

(b)

```
VVoltageSource_1 from time 0 to 100
Average power consumed -> 1.116564e-015 watts
Max power 2.524444e-004 at time 8.09794e-008
Min power 0.000000e+000 at time 0

VVoltageSource_2 from time 0 to 100
Average power consumed -> 1.440304e-015 watts
Max power 2.727941e-004 at time 6.08697e-008
Min power 0.000000e+000 at time 0
```

(c)

Fig 4 : Shows (a) Area (b) Delay (c) Power

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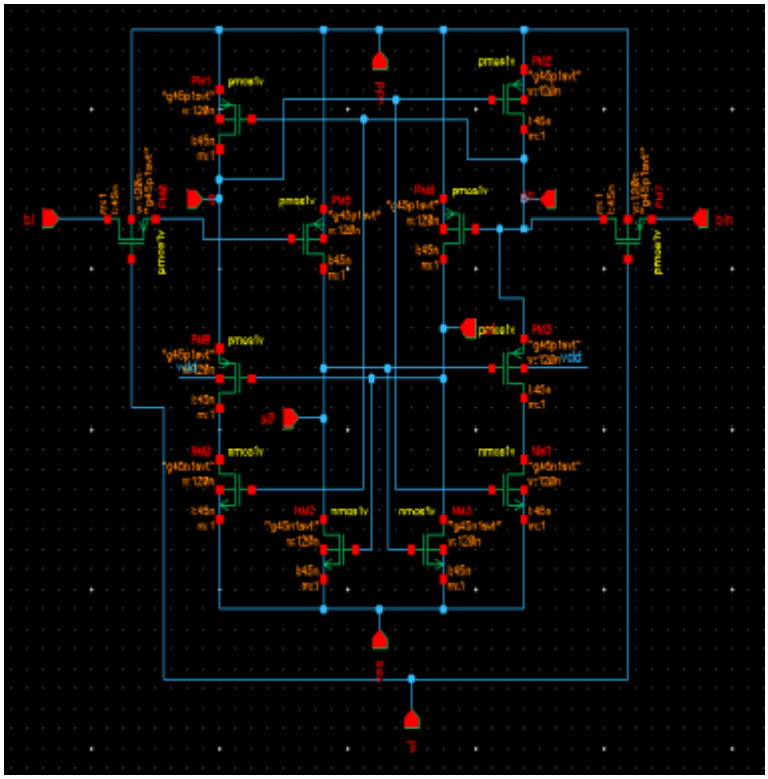
Proposed Method Layout:



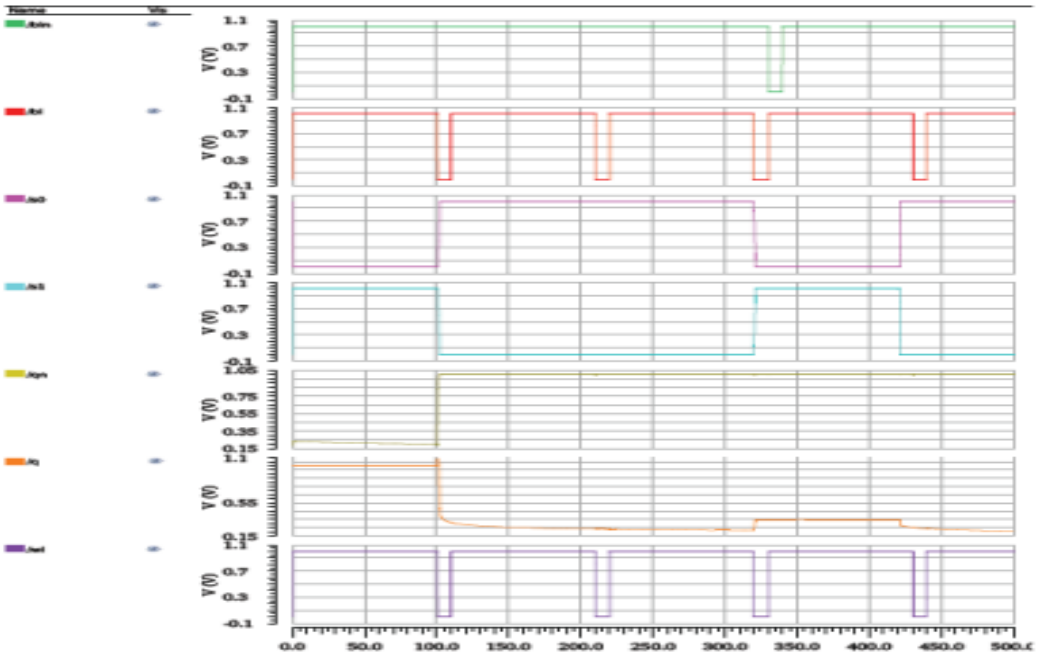


Fig 5 : Shows Output waveforms

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```
Device and node counts:
             MOSFETs -       11
   MOSFET geometries -        2
     Voltage sources -        3
         Subcircuits -        0
   Model Definitions -        2
     Computed Models -        2
   Independent nodes -       53
      Boundary nodes -        4
         Total nodes -       57
```

(a)

```
Parsing                    0.01 seconds
Setup                      0.05 seconds
DC operating point         0.07 seconds
Transient Analysis         0.03 seconds
Overhead                   0.91 seconds
-----------------------------------------
Total                      1.07 seconds
```

(b)

```
Power Results

VVoltageSource_3 from time 0 to 100
Average power consumed -> 5.594084e-011 watts
Max power 2.061770e+000 at time 8.025e-008
Min power 8.198842e-003 at time 3.20774e-008
```

(c)

Fig 6 : Shows Proposed Method (a) Area (b) Delay (c) Power

V.CONCLUSION

To reduce the effects of soft errors in commercial 65 nm CMOS technology, an unique 12T RHBD memory cell is developed. The suggested memory cell's key contribution is its ability to effectively guard against multiple-node upsets, in addition to its tolerance for single-node upsets. The SEU resilience of the process is further confirmed by 1000 MC simulations, the results of which show that process change has no effect on the robustness of the SEU. One possible drawback to the proposed 12T memory cell is that it has a longer read access time than current memory technologies, which might slow down some high-speed applications. However, memory size, resilience, and dependability may be more significant in mission-critical aircraft applications. Therefore, the RHBD 12T memory cell suggested in this study is a good design for radiation robustness in comparison to other state-of-the-art hardened memory cells, as seen from the perspective of a critical application designer. As a result, the general approach to improving this paper is to focus on minimising its space overhead while simultaneously increasing its time performance.

Since the BTI causes a change in the transistor's Vth value, it is one of the most difficult reliability issues to solve at the Nano scale. Degradation of SNM occurs due to a Vth shift in the transistors of SRAMs. In this study, we present a sensor that can detect BTI deterioration in SRAM cells reliably so that their ageing can be tracked. To this end, it is necessary to monitor the peak of Ivdd/Ignd of the SRAM block during the write operation to get a sense of the NBTI/PBTI-aging of the SRAM cells. The CCVS measures this current and produces an equivalent voltage. The frequency of the VCO's oscillations is determined by the peak of this voltage. The magnitude of the BTI effect may be seen in the frequency shift of the oscillations relative to the reference frequency of a freshly synthesised cell. The BTI status of any given row or even individual cells may be determined by reading the values stored in the SRAM.

FUTURE SCOPE

In harsh environments, general memory cells suffer with soft errors caused due to high energy particles. In order to overcome these soft errors like single event upsets and multiple event upsets, the radiation hardened designs with 10T, 12T and 14T memory cells are used. The performance comparison analysis of single event upsets to multi event upsets, are performed. The use of 10T cell increases the robustness of the memory cell design. Compared all the radiation hardened memory cells, 10T memory cells exhibits less in area, power and delay. A 2 byte RHBD memory is designed using 10T memory cells. This memory architecture can be implemented in any high radiation environment.

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